Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **A1**
2. **B1**
3. **Y1**
4. **Y2**
5. **A2**
6. **B2**
7. **VSS**
8. **A3**
9. **B3**
10. **Y3**
11. **Y4**
12. **A4**
13. **B4**
14. **VDD**

**.037”**

**.049”**

**11**

**10**

**2 1 14 13 12**

**5 6 7 8 9**

**3**

**4**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: C**

**APPROVED BY: DK DIE SIZE .037” X .049” DATE: 9/6/18**

**MFG: NATIONAL THICKNESS .015” P/N: CD4001B**

**DG 10.1.2**

#### Rev B, 7/1